AMENDMENTS TO THE CLAIMS (None)

1. (Previously Amended) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

2. (Previously Amended) The memory cell array of Claim 1 wherein the stacked gates and the select gates are self-aligned relative to each other.

3. (Previously Amended) The memory cell array of Claim 1 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics.

4. (Previously Amended) The memory cell array of Claim 1 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

5. (Previously Amended) The memory cell array of Claim 1 wherein erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates.

6. (Previously Amended) The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

7. (Original) The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the

floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. (Previously Amended) The memory cell array of Claim 1 wherein the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region.

9. (Previously Amended) The memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a first positive voltage is applied to a cell select gate for the selected cell, a voltage higher than the first positive voltage is applied to the source region at the end of the row in which the selected cell is located, a voltage higher than the first positive voltage is applied to the control gate in the selected cell, a voltage higher than the first positive voltage is applied to the select gates for unselected cells, and a voltage higher than the first positive voltage is applied to the control gates in the unselected cells.

10. (Previously Amended) The memory cell array of Claim 1 wherein an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts.

11. (Previously Amended) The memory cell array of Claim 1 wherein an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating.

12. (Previously Amended) The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

13. (Original) The memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

14. Cancelled.

15. (Previously Amended) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source diffusion in the active area with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

16. (Previously Amended) The memory cell array of Claim 15 wherein the select gates are self-aligned to the control and floating gates.

17. (Previously Amended) The memory cell array of Claim 15 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between floating gates and control gates, with the tunnel oxide being thinner than the first and second dielectrics.

18. (Previously Amended) The memory cell array of Claim 15 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

19. (Previously Amended) A NAND flash memory cell array, comprising: a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions.

20. (Previously Amended) The memory cell array of Claim 19 wherein the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other.

21. (Previously Amended) The memory cell array of Claim 19 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between floating gates and control gates, with the tunnel oxide being thinner than the first and second dielectrics.

22. (Previously Amended) The memory cell array of Claim 19 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

23. Cancelled.

24. (Previously Added) A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.